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THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): TAKEHARA	**Patent No.: 7,119,717**
Serial No.: 10/812,311	**Issued: October 10, 2006**
Filed: March 30, 2004	
Title: ENCODER OUTPUT DIVIDER AND R/D CONVERTER	Atty. Dkt.: MINB-02023/A-3194

Commissioner for Patents
Alexandria, VA 22313-1450
Mail Stop: Certificate of Corrections

Date: April 24, 2007

REQUEST FOR CERTIFICATE OF CORRECTION

Sir:

Applicant hereby requests that the above-identified Letters Patent be corrected to include the information in the claims on pages 7 – 10 of the patent. Specifically, claim 2 should be corrected as follows:

2. An encoder output divider according to claim 1, wherein:

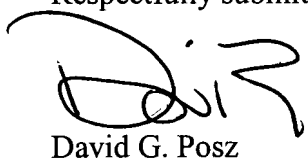
the calculated value includes a rotational speed associated with a resolver; and

the output selector is configured such that when the calculated rotational speed is within a designated range of rotational speeds, the first divided encoded signal is selected for output, and when the calculated rotational speed is outside the designated range of rotational speeds, the encoded signal is selected for output.

Applicants also request that the attached Certificate of Correction be attached to all copies of the Letters Patent.

Although this error is due to the Patent and Trademark Office, no fee is enclosed. However, authorization is hereby given to charge any fee deficiencies or credit any overpayment to Deposit Account 01-0305.

Respectfully submitted,



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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO: 7,119,717
DATED: October 10, 2006
INVENTOR(S): Takao Takehara

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

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Correct claims as follows:

1. An encoder output divider configured to divide an encoded signal, comprising:

a timer configured to measure a first period of the encoded signal;

a divider coupled to the timer and configured to generate a first divided encoded signal having a second period, the second period related to the first period by a multiplication factor of 1/n, where n includes an integer having a value of 2 or more;

a calculator coupled to the divider and the timer and configured to calculate a value based on the measured first period; and

an output selector coupled to the calculator, the divider and the timer and configured such that when the calculated value is within a designated range, the first divided encoded signal is selected for output, and when the calculated value is outside the designated range, the encoded signal is selected for output.

2. An encoder output divider according to claim 1, wherein:

the calculated value includes a rotational speed associated with a resolver; and

the output selector is configured such that when the calculated rotational speed is within a designated range of rotational speeds, the first divided encoded signal is selected for output, and when the calculated rotational speed is outside the designated range of rotational speeds, the encoded signal is selected for output.

3. An encoder output divider according to claim 2, wherein the designated range of rotational speeds includes speeds from 400 rpm to 1200 rpm.

4. An encoder output divider according to claim 1, wherein:

the divider is further configured to generate a second divided encoded signal having the second period and offset in time from the first divided encoded signal by a quarter of the second period; and

the output selector is further configured such that when the calculated value is within the designated range, the first divided encoded signal and the second divided encoded signal are selected for output, and when the calculated value is outside the designated range, the first encoded signal and the second encoded signal are selected for output.

5. A resolver/digital (R/D) converter configured to find an angle of a rotor axis of a resolver based on a sine wave output and a cosine wave output of the resolver, the R/D converter comprising:

a converter configured to convert the sine wave output and cosine wave output of the resolver into an encoded signal;

a timer coupled to the converter and configured to measure a first period of the encoded signal;

a signal generator coupled to the converter and the timer and configured to generate a divided encoded signal having a second period, the second period related to the first period by a multiplication factor of 1/n, where n includes an integer having a value of 2 or more;

a calculator coupled to the signal generator, the converter, and the timer, the calculator configured to calculate the rotational speed of the resolver based on the measured first period of the encoded signal; and

an output selector coupled to the calculator, the signal generator, the converter, and the timer, the output selector configured to select the divided encoded signal for output when the calculated rotational speed of the resolver is within a designated range, and to select the encoded signal for output when the calculated rotational speed is outside the designated range.

6. An R/D converter according to claim 5, wherein the designated range of rotational speeds includes rotational speeds from 400 rpm to 1200 rpm.

7. A resolver/digital (R/D) converter according to claim 5, wherein:

the encoded signal includes a first encoded signal and a second encoded signal each having the first period;

the divided encoded signal includes a first divided encoded signal and a second divided encoded signal each having the second period;

the signal generator is further configured to generate the second divided encoded signal offset in time from the first divided encoded signal by a quarter of the second period; and

the output selector is further configured to select the first divided encoded signal and the second divided encoded signal for output when the calculated rotational speed of the resolver is within a designated range, and to select the first encoded signal and the second encoded signal for output when the calculated rotational speed is outside the designated range.

8. An encoder comprising:

a converter configured to convert a sine wave signal and a cosine wave signal from a resolver into an encoded signal having a first period; and

a digital signal processor (DSP) coupled to the converter, the DSP configured to:

measure the first period of the encoded signal,

generate a divided encoded signal having a second period related to the measured first period by a value of 1/n where n is an integer of 2 or greater,

determine a rotational speed associated with the resolver based on the measured first period, and

provide a selection signal such that when the rotational speed is within a designated range, the selection signal indicates that the divided encoded signal should be output, and when the rotational speed is outside the designated range, the encoded signal should be output, wherein

the divided encoded signal includes a first divided encoded signal and a second divided encoded signal, and

the DSP is further configured to generate the second divided encoded signal offset from the first divided encoded signal by a quarter of the second period and having a period equal to the second period,

the encoder further comprising:

a multiplexer coupled to the DSP and the converter, the multiplexer configured to receive the selection signal and output the first divided encoded and the second divided encoded signal when the rotational speed is within the designated range and output the first and the second encoded signals when the rotational speed is outside the designated range.

9. An encoder-output divider configured to divide an encoded signal, comprising:

a timer configured to measure a first period of the encoded signal; and

a divider coupled to the timer and configured to generate a first divided encoded signal having a second period, the second period related to the first period by a multiplication factor of 1/n, where n includes an integer having a value of 2 or more;

wherein the divider is further configured to generate a second divided encoded signal having

the second period, the second divided encoded signal being offset in time from the first divided encoded signal by a quarter of the second period.

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